CLAIMS:

Sub A2

1. A method of forming a capacitor comprising the following steps:

forming a mass of silicon material over a node location, the mass comprising two forms of silicon;

substantially selectively forming rugged polysilicon from one of the forms of silicon and not from the other of the forms of silicon; and

forming a capacitor dielectric layer and a complementary capacitor plate proximate the rugged polysilicon.

2. The method of claim 1 wherein the two forms of silicon comprise doped silicon and undoped silicon.

3. The method of claim 2 wherein the doped silicon comprises a dopant concentration of at least 5×10^{18} atoms/cm^3 and wherein the undoped silicon comprises a dopant concentration of less than 5×10^{18} atoms/cm^3.

4. The method of claim 2 wherein the doped silicon comprises a dopant concentration of at least 1×10^{19} atoms/cm^3 and wherein the undoped silicon comprises a dopant concentration of less than or equal to 1×10^{18} atoms/cm^3.

Sub. A3

5. A method of forming a capacitor comprising the following steps:

forming a mass of silicon material over a node location, the mass comprising exposed doped silicon and exposed undoped silicon;

substantially selectively forming rugged polysilicon from the exposed undoped silicon and not from the exposed doped silicon; and

forming a capacitor dielectric layer and a complementary capacitor plate proximate the rugged polysilicon and doped silicon.

6. The method of claim 5 wherein the step of forming a mass of silicon material comprises forming a layer of doped silicon between two layers of undoped silicon.

Sub. A4

7. The method of claim 5 further comprising conductively doping the undoped silicon after forming the rugged polysilicon.

8. The method of claim 5 further comprising, after forming the rugged polysilicon, out-diffusing impurity from the doped silicon into the undoped silicon to conductively dope the undoped silicon.

9. The method of claim 5 wherein the step of forming the mass comprises forming the exposed undoped silicon to be substantially amorphous.

10. The method of claim 5 wherein the step of forming the mass comprises forming the exposed doped silicon to be substantially polycrystalline.

Sub. A5

11. A method of forming a capacitor comprising the following steps:

forming an insulative layer over a node location;

forming an opening through the insulative layer to the node location;

forming two forms of silicon within the opening, the two forms of silicon together forming a capacitor storage node;

exposing the two forms of silicon to common subsequent processing conditions which substantially selectively forming rugged polysilicon from one of the exposed two forms of silicon and not from the other of the exposed two forms of silicon;

forming a dielectric layer proximate the storage node; and

forming a cell plate layer proximate the dielectric layer.

12. The method of claim 11 wherein the two forms of silicon comprise doped silicon and undoped silicon.

Sub B6

13. A method of forming a capacitor comprising the following steps: forming an insulative layer over a node location;

forming an opening through the insulative layer to the node location;

forming silicon material within the opening, the silicon material comprising doped silicon and undoped silicon and defining a capacitor storage node;

removing a portion of the insulative layer to expose a sidewall surface of the storage node, the exposed sidewall surface comprising undoped silicon;

forming HSG from the undoped silicon of the exposed sidewall surface;

forming a capacitor dielectric layer proximate the storage node; and

forming a complementary capacitor plate proximate the capacitor dielectric layer.

14. The method of claim 13 wherein the doped silicon comprises polysilicon and the undoped silicon comprises substantially amorphous silicon.

15. The method of claim 13 wherein the step of forming the silicon material comprises forming a layer of doped silicon between two layers of undoped silicon.

16. The method of claim 13 wherein the step of forming the silicon material comprises forming a layer of doped polysilicon between two layers of undoped substantially amorphous silicon.

Sub B7

17. A method of forming a capacitor comprising the following steps:

forming an insulative layer over a node location;

forming an opening through the insulative layer to the node location;

forming an undoped silicon layer within the opening to narrow the opening;

forming a doped silicon layer within the narrowed opening, the undoped silicon layer and doped silicon layer together defining a capacitor storage node;

forming a capacitor dielectric layer proximate the storage node; and

forming a complementary capacitor plate proximate the capacitor dielectric layer.

18. The method of claim 17 wherein the undoped silicon layer comprises substantially amorphous silicon.

19. The method of claim 17 wherein the doped silicon layer comprises polysilicon.

20. The method of claim 17 further comprising:

removing a portion of the insulative layer to expose a sidewall surface of the storage node comprising the undoped silicon layer; and

forming rugged polysilicon from the exposed sidewall surface.

21. The method of claim 17 further comprising:

exposing a surface of the capacitor storage node comprising undoped silicon;

exposing a surface of the capacitor storage node comprising doped silicon; and

substantially selectively forming HSG polysilicon from the exposed capacitor storage node surface comprising undoped silicon and not from the exposed capacitor storage node surface comprising doped silicon.

22. The method of claim 21 wherein the formation of the rugged polysilicon comprises:

in situ HF cleaning of the exposed sidewall surface;

seeding the exposed sidewall surface with polysilicon; and

annealing the seeded sidewall surface at about 560° C for about 20 minutes.

23. The method of claim 21 wherein the formation of the rugged polysilicon comprises:

in situ HF cleaning of the exposed sidewall surface;

seeding the exposed sidewall surface with polysilicon;

annealing the seeded sidewall surface at about 560° C for about 20 minutes; and

a polysilicon etch after the annealing to remove any monolayers of silicon.

Sub. A8

24. A method of forming a capacitor comprising the following steps: forming an insulative layer over a node location;

forming an opening through the insulative layer to the node location;

forming a first undoped silicon layer within the opening to narrow the opening;

forming a doped silicon layer within the narrowed opening to further narrow the opening;

forming a second undoped silicon layer within the further narrowed opening; the first undoped silicon layer, second undoped silicon layer and doped silicon layer together defining a capacitor storage node;

removing a portion of the insulative layer to expose a sidewall surface of the storage node comprising the first undoped silicon layer;

forming rugged polysilicon on the exposed sidewall surface;

forming a dielectric layer proximate the storage node; and

forming a cell plate layer proximate the dielectric layer.

25. The method of claim 24 further comprising:

exposing a surface of the capacitor storage node comprising the second undoped silicon layer;

exposing a surface of the capacitor storage node comprising the doped silicon layer; and

substantially selectively forming HSG polysilicon from the exposed capacitor storage node surface comprising undoped silicon and not from the exposed capacitor storage node surface comprising doped silicon.

add A9

26. A method of forming a DRAM array comprising the following steps:

defining a first node location, a second node location and a third node location; the second node location being electrically coupled to the first node location through a first transistor gate; the second node location being electrically coupled to the third node location through a second transistor gate;

forming an electrically insulative layer over the node locations;

removing portions of the electrically insulative layer to form a first opening, a second opening, and a third opening; the first, second and third openings extending to the first, second and third node locations, respectively;

forming an undoped silicon layer within the first, second and third openings to narrow the first, second and third openings;

forming a doped silicon layer within the narrowed openings; the undoped silicon layer and the doped silicon layer within the first opening together defining a first storage node; the undoped silicon layer and the doped silicon layer within the third opening together defining a second storage node; the undoped silicon layer and the doped silicon layer within the second opening together defining a conductive contact;

removing a portion of the electrically insulative layer to expose sidewall surfaces of the first storage node, the second storage node and the conductive contact;

forming rugged polysilicon on the exposed sidewall surfaces;

forming a dielectric layer proximate the first and second storage nodes;

forming a cell plate layer proximate the dielectric layer; the cell plate layer, dielectric layer and first storage node together defining a first capacitor; the cell plate layer, dielectric layer and second storage node together defining a second capacitor; and

forming a bitline electrically connected to the conductive contact; the conductive contact and first capacitor together defining a first DRAM cell; the conductive contact and second capacitor together defining a second DRAM.

27. The method of claim 26 wherein the exposed sidewall surfaces comprise undoped silicon, the method further comprising:

exposing a surface of the first storage node comprising the doped silicon layer;

exposing a surface of the second storage node comprising the doped silicon layer; and

substantially selectively forming HSG polysilicon from the exposed first and second storage node surfaces comprising undoped silicon and not from the exposed first and second storage node surfaces comprising doped silicon.

28. The method of claim 26 wherein the doped and undoped silicon layers are formed over the insulative layer, the method further comprising polishing the doped and undoped silicon layers to remove the doped and undoped silicon layers from over the electrically insulative layer.

29. A method of forming a DRAM array comprising the following steps:

defining a first node location, a second node location and a third node location; the second node location being electrically coupled to the first node location through a first transistor gate; the second node being electrically coupled to the third node location through a second transistor gate;

forming an electrically insulative layer over the node locations;

removing portions of the electrically insulative layer to form a first opening, a second opening, and a third opening; the first, second and third openings extending to the first, second and third node locations, respectively;

forming an undoped silicon layer within the first, second and third openings to narrow the first, second and third openings;

forming a doped silicon layer within the narrowed first, second and third openings to further narrow the first, second and third openings;

forming a second undoped silicon layer within the further narrowed first, second and third openings; the first undoped silicon layer, second undoped silicon layer and doped silicon layer within the first opening together defining a first storage node; the first undoped silicon layer, second undoped silicon layer and doped silicon layer within the third opening together defining a second storage node; the first undoped silicon layer, second undoped silicon layer and doped silicon layer within the second opening together defining a conductive contact;

removing a portion of the electrically insulative layer to expose sidewall surfaces of the first and second storage nodes and of the conductive contact;

forming rugged polysilicon on the exposed sidewall surfaces;

forming a dielectric layer proximate the first and second storage nodes;

forming a cell plate layer proximate the dielectric layer; the cell plate layer, dielectric layer and first storage node together defining a first capacitor; the cell plate layer, dielectric layer and second storage node together defining a second capacitor; and

forming a bitline electrically connected to the conductive contact; the conductive contact and first capacitor together defining a first DRAM cell; and the conductive contact and second capacitor together defining a second DRAM cell.

30. The method of claim 29 wherein the exposed sidewall surfaces comprise the first undoped silicon layer, the method further comprising:

exposing a surface of the first storage node comprising the second undoped silicon layer;

exposing a surface of the first storage node comprising the doped silicon layer;

exposing a surface of the second storage node comprising the second undoped silicon layer;

exposing a surface of the second storage node comprising the doped silicon layer; and

substantially selectively forming HSG polysilicon over the exposed first and second storage node surfaces comprising undoped silicon and not over the exposed first and second storage node surfaces comprising doped silicon.

31. The method of claim 29 wherein the doped and undoped silicon layers are formed over the insulative layer, the method further comprising polishing the doped and undoped silicon layers to remove the doped and undoped silicon layers from over the electrically insulative layer.

32. A method of forming a monolithic integrated circuit comprising the following steps:

fabricating integrated circuitry over a portion of a semiconductor substrate, the integrated circuitry comprising elements including transistors, capacitors and resistive elements;

the fabrication of at least one of the capacitors comprising the following steps:

forming a mass of silicon material over a node location, the mass comprising exposed doped silicon and exposed undoped silicon;

substantially selectively forming rugged polysilicon from the exposed undoped silicon and not from the exposed doped silicon; and

forming a capacitor dielectric layer and complementary capacitor plate proximate the rugged polysilicon and doped silicon.

33. The method of claim 32 wherein the monolithic integrated circuit is fabricated as part of a microprocessor circuit.

34. The method of claim 32 wherein the monolithic integrated circuit is fabricated as part of a microprocessor circuit and wherein the capacitor is integrated into a DRAM cell.

35. A capacitor comprising:

a first capacitor plate;

a second capacitor plate;

a capacitor dielectric layer intermediate the first and second capacitor plates; and

at least one of the first and second capacitor plates comprising a surface against the capacitor dielectric layer and wherein said surface comprises both doped rugged polysilicon and doped non-rugged polysilicon.

36. A capacitor comprising:

a capacitor storage node having a rugged-polysilicon-comprising lateral surface and a top surface, a predominate portion of the top surface not comprising rugged polysilicon;

a dielectric layer proximate the capacitor storage node; and

a cell plate layer proximate the dielectric layer.

37. The capacitor of claim 36 wherein the storage node further comprises a container shape and an interior rugged-polysilicon-comprising surface.

38. A DRAM array comprising:

a first node location, a second node location and a third node location associated with a semiconductor substrate;

a first transistor gate electrically coupling the first node location to the second storage node location;

a second transistor gate electrically coupling the third node location to the second node location;

an electrically insulative layer over the node locations;

a first storage node extending through the electrically insulative layer to the first node location, the first storage node having a rugged-polysilicon-comprising lateral surface and top surface, a predominate portion of the top surface not comprising rugged polysilicon;

a second storage node extending through the electrically insulative layer to the third node location, the second storage node having a rugged-polysilicon-comprising lateral surface and a top surface, a predominate portion of the top surface not comprising rugged polysilicon;

a conductive contact extending through the electrically insulative layer to the second node location;

a first dielectric layer proximate the first storage node;

a first cell plate layer proximate the first dielectric layer; the first cell plate layer, first dielectric layer and first storage node together defining a first capacitor;

a second dielectric layer proximate the second storage node;

a second cell plate layer proximate the second dielectric layer; the second cell plate layer, second dielectric layer and second storage node together defining a second capacitor; and

a bitline electrically connected to the conductive contact; the conductive contact and first capacitor together defining a first DRAM cell electrically connected to the bitline; the conductive contact and second capacitor together defining a second DRAM cell electrically connected to the bitline.

39. The DRAM array of claim 38 wherein the conductive contact has a rugged-polysilicon-comprising lateral surface.

40. The DRAM array of claim 38 wherein the first and second capacitor storage nodes comprise container shapes and further include interior rugged-polysilicon-comprising surfaces.

41. A monolithic integrated circuit comprising:

fabricated circuitry over a semiconductor substrate, the integrated circuitry comprising elements including transistors, capacitors and resistive elements;

at least one of the capacitors comprising:

a first capacitor plate;

a second capacitor plate;

a capacitor dielectric layer intermediate the first and second capacitor plates; and

at least one of the first and second capacitor plates comprising a surface against the capacitor dielectric layer and wherein said surface comprises both doped rugged polysilicon and doped non-rugged polysilicon.

42. The monolithic integrated circuit of claim 41 wherein the monolithic integrated circuit is part of a microprocessor circuit.

43. The monolithic integrated circuit of claim 41 wherein the monolithic integrated circuit is part of a microprocessor circuit and wherein the at least one capacitor is incorporated into a DRAM cell.